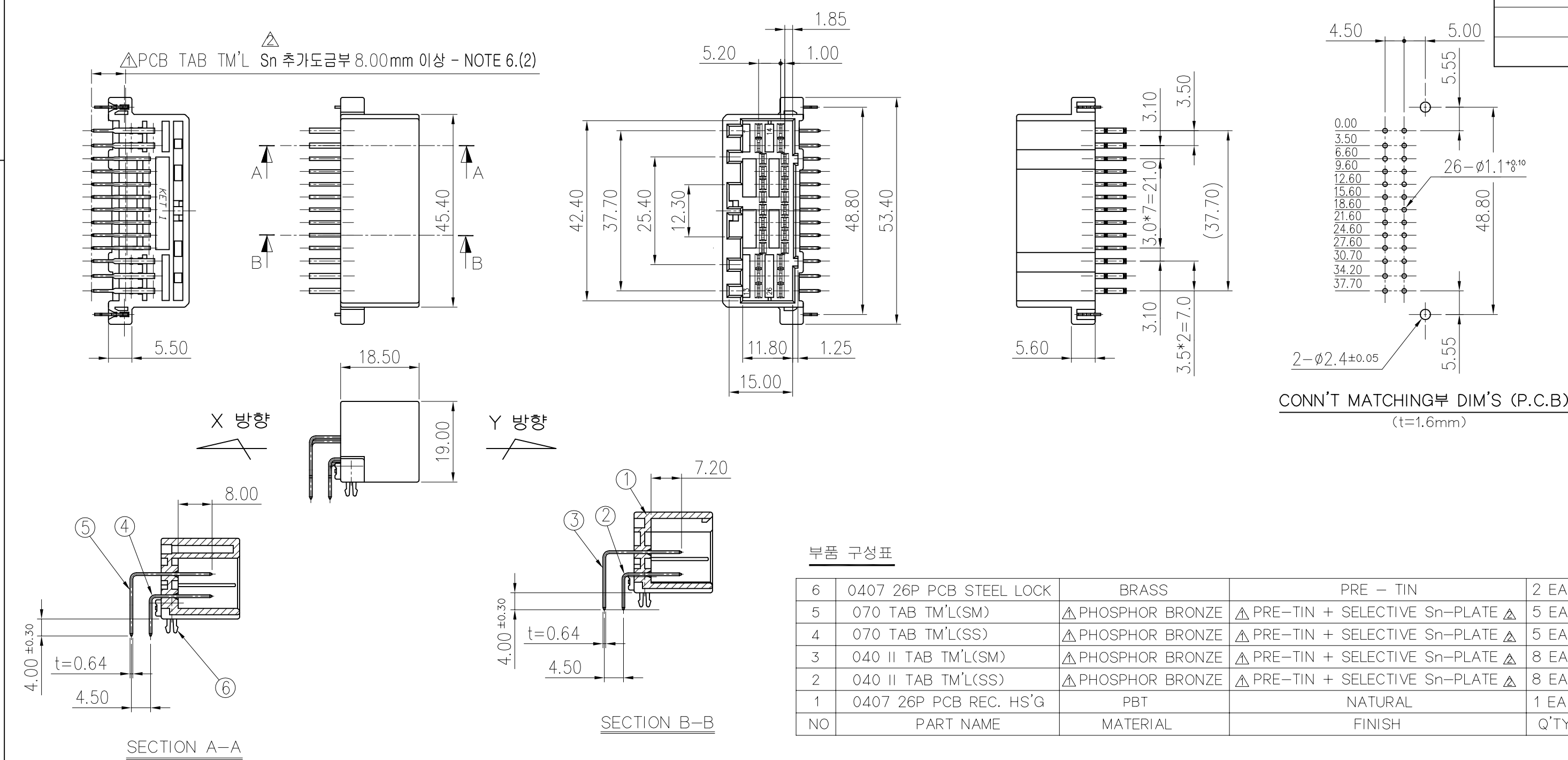




NOTE

1. 지시하지 않은 반경 R은 0.5로 한다

2. 기능상 유해한 BURR등 변형이 없을것.

3. 적용 PLUG HOUSING : MG611336

4. 본 제품은 ES-91500 항을 만족할것.

5. TERMINAL 고착력 : "X"방향 6 Kgf 이상

"Y"방향 2 Kgf 이상

△6. 도금사항

(1) CONTACT부 - Sn 선도금 : PRESS 타발전 REFLOW처리 되 있을것.

광택 Sn : 0.8~1.8 μm

△ (2) SOLDERING부(TM'L 끝단 8mm 이상) - Sn 선도금 + Sn 추가도금

△ 광택 Sn : 0.8~1.8 μm + 광택 Sn 7~15 μm

△ (3) 상기 (2)항 PRESS 파단면 - Sn 추가도금

△ 광택 Sn 7~15 μm

(4) PCB-LOCK부 - Sn 선도금 : PRESS 타발전 REFLOW처리 되 있을것.

광택 Sn : 0.8~1.8 μm , 동하지 0.3~0.8 μm

NOTE

1. UNLESS OTHERWISE SPECIFIED ALL RADII TO BE 0.5 RADIOUS

2. MUST BE FREE OF FLASH, SINK AND IMPERFECTION THAT AFFECT FUNCTION.

3. MATING PLUG HOUSING : MG611336

4. THE PRODUCT MUST MEET SPEC' NO. ES-91500

5. TERMINAL RETENSION FORCE: "X" DIRECTION 6 Kgf MIN

"Y" DIRECTION 2 Kgf MIN

△6. PLATING SPECIFICATION

(1) CONTACTED AREA - PRE-TIN : REFLOW PROCESS BEFORE STAMPING.

GROSS TIN PLATE 0.8~1.8 μm

△ (2) SOLDERED AREA(TM'L END OVER 8mm) - PRE-TIN + Sn PLATING

△ GROSS TIN PLATE 0.8~1.8 μm + GROSS Sn 7~15 μm

△ (3) STAMPED AREA OF (THE ABOVE STATEMENTS (2)) - Sn PLATING

△ GROSS Sn 7~15 μm

(4) PCB-LOCK PARTS - PRE-TIN : REFLOW PROCESS BEFORE STAMPING.

GROSS TIN PLATE 0.8~1.8 μm , GROUND BRONZE PLATE : 0.3~0.8 μm

부품 구성표

6	0407 26P PCB STEEL LOCK	BRASS	PRE - TIN	2 EA
5	070 TAB TM'L(SM)	△ PHOSPHOR BRONZE	△ PRE-TIN + SELECTIVE Sn-PLATE △	5 EA
4	070 TAB TM'L(SS)	△ PHOSPHOR BRONZE	△ PRE-TIN + SELECTIVE Sn-PLATE △	5 EA
3	040 II TAB TM'L(SM)	△ PHOSPHOR BRONZE	△ PRE-TIN + SELECTIVE Sn-PLATE △	8 EA
2	040 II TAB TM'L(SS)	△ PHOSPHOR BRONZE	△ PRE-TIN + SELECTIVE Sn-PLATE △	8 EA
1	0407 26P PCB REC. HS'G	PBT	NATURAL	1 EA
NO	PART NAME	MATERIAL	FINISH	Q'TY

ISSUE MARK

						MATERIAL	SEE TABLE	KET KOREA ELECTRIC ENGINEERED TERMINAL CO., LTD.	
						FINISH	SEE TABLE		
						WIRE RANGE		CLASS	0407
						INSULATION		TYPE	HYBRID
LTR	REVISION RECORD		DR.	CHK.	APP.	DATE	TOLERANCE EXCEPT AS NOTED ±0.2	SCALE 1/1	PART NO. MG643336
DR.	SHIN '04.02.23.		CHK.	BIN '04.02.23.			PART NAME		
CHK.	2/24		APP.	2/24			0407 26P PCB CONN'T(HZT-PCB LOCK)		